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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new non-provisional applications under 37 CFR 1.53(b)

Attorney Docket No. 42390.P7112 Total Pages 2

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ADDRESS TO: **Assistant Commissioner for Patents**
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APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 11)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 3)

4. ____ Oath or Declaration (Total Pages________)
   a. ___ Newly Executed (Original or Copy)
   b. ___ Copy from a Prior Application (37 CFR 1.63(d))
   (for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**
   i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ____ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ____ Microfiche Computer Program (Appendix)

7. ____ Nucleotide and/or Amino Acid Sequence Submission

(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ____ Assignment Papers (cover sheet & documents(s))
9. ____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
   ____ b. Power of Attorney
10. ____ English Translation Document (if applicable)
11. ____ a. Information Disclosure Statement (IDS)/PTO-1449
    ____ b. Copies of IDS Citations
12. ____ Preliminary Amendment
13. X Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. ____ a. Small Entity Statement(s)
    ____ b. Statement filed in prior application, Status still proper and desired
15. ____ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. Other: ______________________

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
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of prior application No: ____________

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Application for United States Letters Patent

for

Input-Output Bus Interface

by

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"Express Mail" mailing label number: EL431888785US
Date of Deposit: Nov. 30, 1999
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Field

The present invention relates to electronic systems, and more particularly, to a bus.

Background

A GTL (Gunning Transceiver Logic) bus is well-known, where an example of an electronic system utilizing a GTL bus having nMOSFET (n-Metal Oxide Semiconductor Field Effect Transistor) driver **102** is illustrated in Fig. 1. In the example of Fig. 1, two agents are connected to transmission line **104** to receive signals from nMOSFET driver **102**. An agent may be a microprocessor, memory device, or any other electronic device for sending or receiving signals along transmission line **104**. Resistors R_T are termination resistors to reduce reflections at the ends of transmission line **104**, and are connected to a voltage source providing a termination voltage V_{TT}. Resistor R_{ESD} is a resistor to reduce the probability of electrostatic discharge damage to nMOSFET driver **102**, and may not be needed for some applications. The gate of nMOSFET driver **102** is driven according to a digital data signal so as to switch nMOSFET driver **102** ON and OFF to drive transmission line **104**.

The ideal (quiescent or steady state) voltage of transmission line **104** is in the range $[V_{TT} - V_{SW}, V_{TT}]$, where the voltage swing V_{SW} is given by $V_{SW} = V_{TT}[(R_T/2)/(R_{ONn} + R_{ESD} + R_T/2)]$ and where R_{ONn} is the ON resistance of nMOSFET driver **102**. Because of impedance mismatch due to mismatches between nMOSFET driver **102**, termination resistor R_T, and transmission line **104**, as well as stubs **106** and other artifacts, the actual signal voltage propagating along transmission line **104** will have over-shoots and under-shoots outside the ideal or quiescent voltage range. Note that in the above lumped-parameter equation for V_{SW}, the resistance R_{ESD} adds to the resistance R_{ONn}. When R_{ESD} is present, nMOSFET driver **102** needs to be designed with smaller R_{ONn} than when R_{ESD} is not present in order to maintain the same voltage swing on transmission line **104**. However, reducing R_{ONn} increases the size of nMOSFET driver **102**, which increases the impedance mismatch.

In addition to distributing the core voltage V_{CC} in an electronic system, GTL busses also require distributing the termination voltage V_{TT}, which may result in added system cost due to extra motherboard power planes, wiring, pins, etc. Furthermore, with

new process technologies allowing for smaller core voltages than in the past, signal overshoots above V_{TT} may be too large for the oxide thickness of new process technologies. This problem may be alleviated by lowering the termination voltage, but then the voltage range $[V_{TT} - V_{SW}, V_{TT}]$ of transmission line **104** will be shifted, which may require a re-design of agents connected to the transmission line. Embodiments of the present invention address some or all of these problems.

Summary

Embodiments of the present invention are directed to a bus in which a terminated transmission line is excited by a pMOSFET, where the transmission line is terminated by connecting at least one termination device between the transmission line and ground. In one embodiment, the pMOSFET has its drain connected to the transmission line and its source biased to a core voltage V_{CC}.

Brief Description of the Drawings

Fig. 1 illustrates a prior art GTL bus.

Fig. 2 illustrates an exemplary bus according to the present invention.

Fig. 3 illustrates another exemplary bus according to the present invention.

Detailed Description of Embodiments

An embodiment of the present invention is illustrated in Fig. 2. In Fig. 2, pMOSFET driver (pullup) **202** drives transmission line **204** according to a data signal applied to its gate. The source of pMOSFET driver **202** is at a voltage V_{CC}. V_{CC} may, but need not be, a processor core voltage. Resistors R_T provide termination to transmission line **204** so as to reduce reflections and provide a pulldown to substrate voltage V_{SS}. The substrate voltage V_{SS} may also be termed a ground voltage, and the terms ground and substrate may be used interchangeably.

In practice, pMOSFET driver **202** may actually comprise a plurality of pMOSFETs coupled in parallel, where some subset of the plurality of pMOSFETs have their gates enabled to be responsive to the data signal. In this way, the effective ON resistance of pMOSFET driver **202** may be adjusted by proper choice of the enabled subset. It is therefore to be understood in this specification and the following claims that a pMOSFET driver may also include a plurality of parallel coupled pMOSFETs in which all or some proper subset of the plurality are enabled.

By terminating transmission line **204** to V_{SS}, a separate voltage source for V_{TT} is not needed as in some prior art busses. Furthermore, the ideal voltage range of transmission line **204** is $[V_{SS}, V_{SS} + V_{SW}]$, where the swing voltage V_{SW} is given by $V_{SW} = V_{CC}[(R_T/2/(R_{ONp} + R_T/2)]$ and where R_{ONp} is the ON resistance of pMOSFET driver **202**. The ideal voltage range is referenced to V_{SS}, and thus embodiments of the present invention may be better suited to bridging different process technologies than prior art busses.

For many practical situations, the embodiment of Fig. 2 exhibits some other advantages over the embodiment of Fig. 1. For example, when the voltage swings of the embodiments of Figs. 1 and 2 are equal, it is found that the driver of the present embodiment may be better matched to the transmission line characteristic impedance. As a specific example, consider the case in which a 60Ω transmission line is terminated at both ends with 60Ω resistors, and where the voltage swing is 1.0V. For an embodiment of the present invention according to Fig. 2, the output impedance of pMOSFET **202** is 15Ω if V_{CC} = 1.5V. However, for the example of prior art Fig. 1, the sum of the output impedance of nMOSFET **102** with resistor R_{ESD} is 15Ω if V_{TT} = 1.5V. Since $R_{ESD} > 0$, the output impedance of nMOSFET **102** is less than 15Ω, and thus there is greater mismatch than in the embodiment of Fig. 2.

Another advantage of some of the embodiments is that to maintain the same voltage swing, pMOSFET **202** may be similar or smaller in size than nMOSFET **102** without sacrificing driver strength. Also, because pMOSFETs are less susceptible to electrostatic discharge damage, for many applications an electrostatic discharge resistor is not needed for pMOSFET driver **202**. This allows greater flexibility in its manufacturing process. Furthermore, the use of pMOSFETs with an n-well process may be advantageous in that substrate noise may be reduced, which may be particularly advantageous for so-called systems-on-chip designs.

The embodiment of Fig. 2 may be modified in various ways. For example, termination resistors R_T may be replaced with on-chip nMOSFETs. Note that adding electrostatic discharge resistors R_{ESD} to such nMOSFETs not only provide the function of reducing the probability of electrostatic discharge, but they also linearize the effective

resistance termination of the nMOSFETs in combination with the resistors R_{ESD} so as to provide better termination of the transmission line.

Another embodiment of the present invention is provided in Fig. 3, which is applicable to high speed, point-to-point busses in which it is particularly advantageous for a driver's impedance to be matched to a transmission line. However, it is not necessary for the driver's impedance to be matched to the transmission line. In Fig. 3, in addition to pMOSFET driver **202** and transmission line **204**, is nMOSFET driver **302** and combinational logic circuit **304**. nMOSFET driver **302** is shown as comprising a plurality of nMOSFETs **305** having gates connected to output ports **306** of combinational logic circuit **304**. The input port **308** of combinational logic circuit **304** is responsive to the same digital data signal that drives the gate of pMOSFET driver **202**. It is to be understood in this specification and the following claims that a nMOSFET driver may also include a plurality of parallel coupled nMOSFETs in which all or some proper subset of the plurality are enabled.

The input-output relationship of combinational logic circuit **304** is such that when input port **308** is LOW, a subset of nMOFETs **305** is switched ON so that the parallel combination of the ON resistance of nMOSFET driver **302** with the ON resistance of pMOSFET driver **202** is substantially matched to the characteristic impedance of transmission line **204**; whereas when input port **308** is HIGH, the effective ON resistance of nMOSFET driver **302** is substantially matched to the characteristic impedance of transmission line **204**. In this way, the impedance of the combination of pMOSFET driver **202** and nMOSFET driver **302** is matched to transmission line **204**.

The embodiment of Fig. 3 may also be used in a differential signaling scheme, where in addition to the circuit of Fig. 3 another circuit identical to that of Fig. 3 is also employed but in which it is driven by a data signal complementary to the data signal that drives the circuit of Fig. 3.

Various modifications may be made to the disclosed embodiments without departing from the scope of the invention as claimed below.

What is claimed is:

1. A bus comprising:

a transmission line;

a pMOSFET driver to drive the transmission line, the pMOSFET driver having a source connected to a voltage source so as to be biased to a voltage V_{CC}; and

at least one termination device connecting the transmission line to ground.

2. The bus as set forth in claim 1, wherein the voltage V_{CC} is a core voltage.

3. The bus as set forth in claim 1, wherein each at least one termination device comprises a resistor connecting the transmission line to ground.

4. The bus as set forth in claim 1, wherein each at least one termination device comprises an nMOSFET coupling the transmission line to ground.

5. The bus as set forth in claim 1, wherein each at least one termination device is connected to the transmission line so as to provide a quiescent voltage of V_{SS} if the pMOSFET driver is OFF.

6. The bus as set forth in claim 5, wherein the voltage V_{CC} is a core voltage.

7. The bus as set forth in claim 1, the transmission line having two ends, wherein the at least one termination device comprises two resistors, each resistor connecting one end of the transmission line to ground, wherein the pMOSFET has a drain connected to the transmission line.

8. An electronic system comprising:

an integrated circuit having a substrate voltage V_{SS} and a voltage V_{CC};

a voltage source to provide the voltage V_{CC};

a transmission line having an end;

an agent connected to the transmission line;

a pMOSFET driver connected to the transmission line to communicate with the agent, the pMOSFET driver having a drain connected to the transmission line and having a source connected to the voltage source so as to be biased at the voltage V_{CC}; and

a termination device connected to the end of the transmission line to reduce signal reflection.

9. The electronic system as set forth in claim 8, wherein the voltage V_{CC} is a core voltage.

10. The electronic system as set forth in claim 8, wherein the termination device is connected to the transmission line so as to provide a quiescent voltage substantially equal to V_{SS} if the pMOSFET driver is OFF.

11. The electronic system as set forth in claim 10, wherein the voltage V_{CC} is a core voltage.

12. The electronic system as set forth in claim 8, wherein the termination device comprises at least one resistor connected to ground.

13. The electronic system as set forth in claim 8, wherein the termination device comprises at least one nMOSFET having a source connected to ground.

14. A bus comprising:

a transmission line;

a pMOSFET driver having a drain connected to the transmission line and a source at a voltage V_{CC}; and

at least one termination device connecting the transmission line to ground.

15. The bus as set forth in claim 14, wherein the voltage V_{CC} is a core voltage.

16. A method to provide electrical communication to a first agent and to a second agent via a transmission line, the first agent having a voltage V_{CC} and a substrate voltage V_{SS}, the method comprising:

exciting the transmission line in response to the first agent by switching ON a pMOSFET having a drain connected to the transmission line and a source at the voltage V_{CC};

reducing signal reflection from an end of the transmission line by providing at least one termination device connecting the transmission line to a source providing the substrate voltage V_{SS}; and

exciting the transmission line in response to the first agent by switching OFF the pMOSFET.

17. The method as set forth in claim 16, wherein the voltage V_{CC} is a core voltage.

18. A bus comprising:

a transmission line;

a pMOSFET driver to drive the transmission line, the pMOSFET driver having a source connected to a voltage source so as to be biased to a voltage V_{CC};

a nMOSFET driver coupled to the transmission line, the nMOSFET driver having a source at a substrate voltage V_{SS}; and

a combinational logic circuit coupled to the nMOSFET driver.

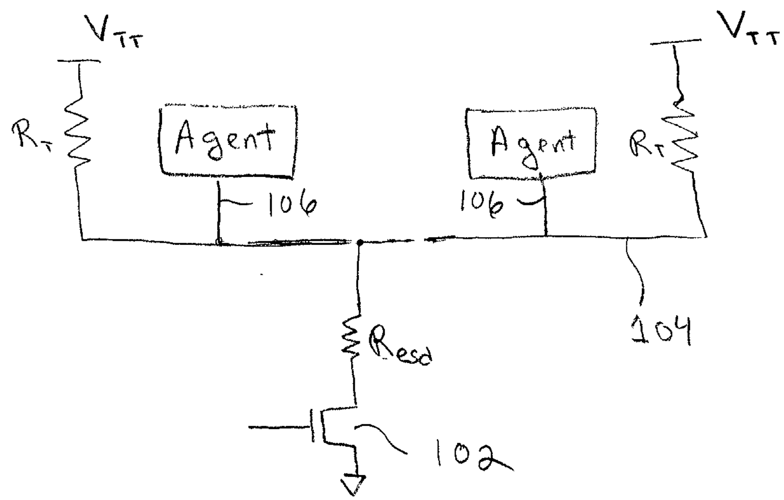
19. The bus as set forth in claim 18, wherein the combinational logic circuit is coupled to the nMOSFET driver so that the nMOSFET driver has a first ON resistance when the pMOSFET driver is ON and a second ON resistance when the pMOSFET driver is OFF, wherein the first and second ON resistances are not equal to each other.

20. The bus as set forth in claim 18, wherein the voltage V_{CC} is a core voltage.

21. The bus as set forth in claim 18, wherein the pMOSFET driver and nMOSFET in combination have an impedance substantially matched to the transmission line if both the pMOSFET driver and nMOSFET driver are switched ON, and wherein the nMOSFET has an impedance substantially matched to the transmission line if the pMOSFET driver is switched OFF.

Abstract

A bus in which a transmission line is excited by a pMOSFET having a drain connected to the transmission line and having a source at a core voltage V_{CC}, and in which the transmission line is terminated by a device connected to ground.



(Prior Art)

Fig. 1

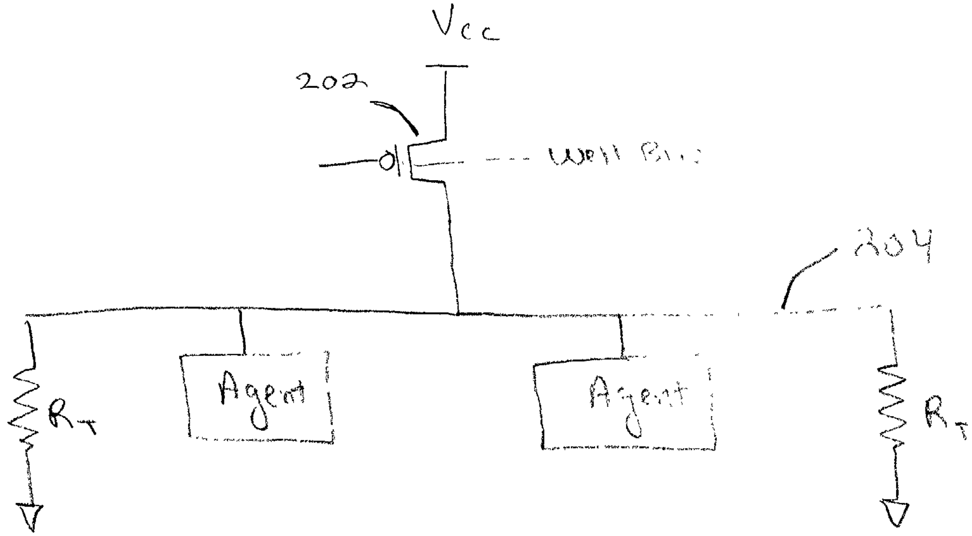


Fig. 2

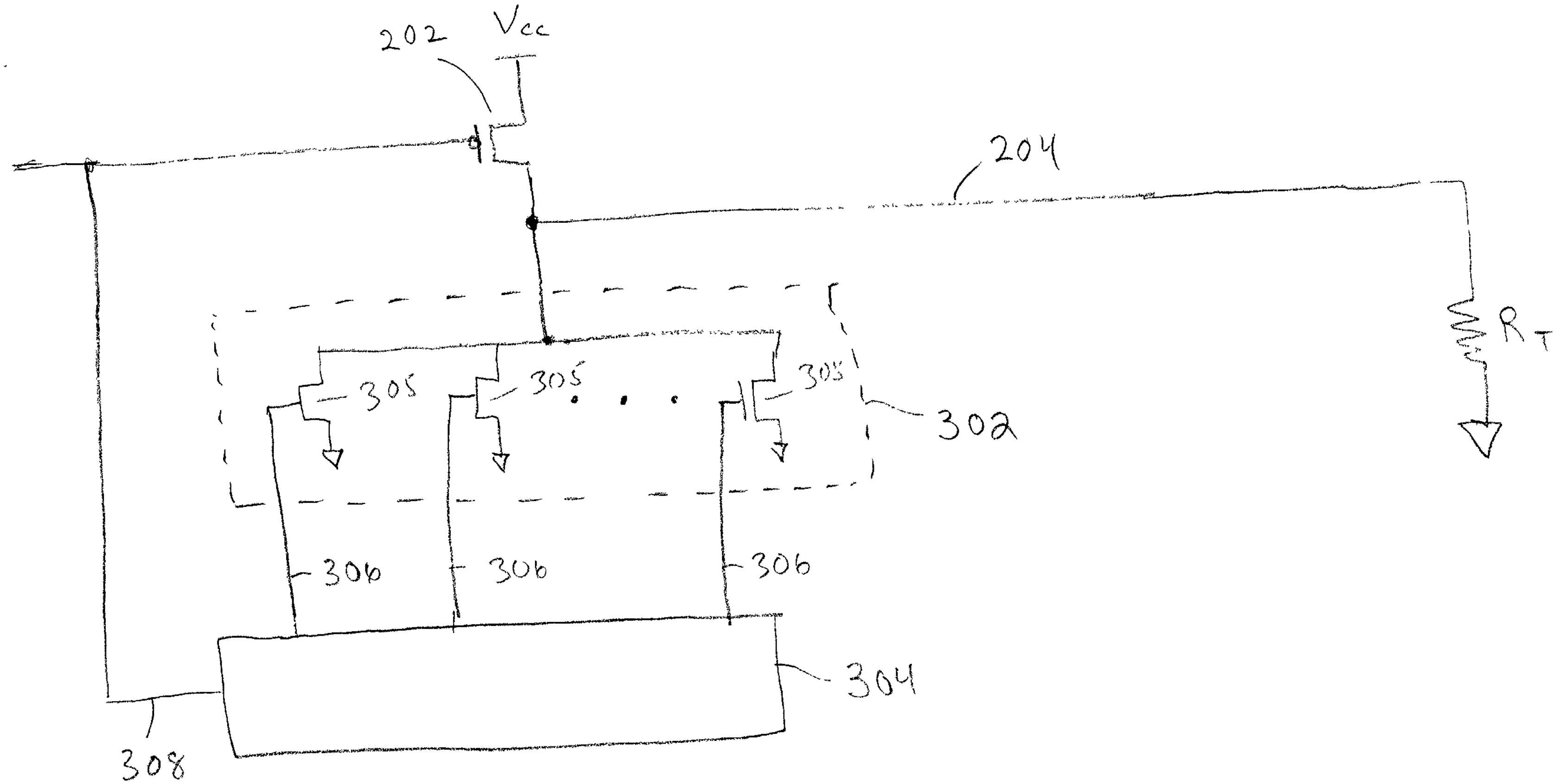


Fig. 3